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Applicants: Alcoe *et al.*	Examiner: Mitchell, James M.
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For: **HYPERBGA BUILDUP LAMINATE**	

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Commissioner for Patents
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Sir:

This present paper is being filed as a corrected response to the Office Action mailed July 5, 2002. This present paper is in response to the Notice of Non-Compliant Amendment mailed October 23, 2002. The only difference between this present paper and the previous response filed by Applicants on October 7, 2002 is that this present response provides both a clean version and a marked-up version of the complete replacement paragraphs referred to in the Notice of Non-Compliant Amendment mailed October 23, 2002.

Applicants respectfully request that the above-identified application be reconsidered in view of the Amendments and Remarks that follow, that each of the presently pending claims be allowed, and that the application be passed to issue.

AMENDMENT

In The Specification

The paragraphs encompassing page 1, line 12 - page 2, line 16 has been amended as marked up in Appendix A:

The present invention provides an electronic structure, comprising:

an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

a redistribution structure having N dielectric layers denoted as dielectric layers 1, 2, ..., N, N metal planes denoted as metal planes 1, 2, ..., N, and a microvia structure through the N dielectric layers, wherein N is at least 2, wherein dielectric layer 1 is on the first surface of the substrate and on the metallic plane, wherein metal plane J is on dielectric layer J for J =1, 2, ..., N, wherein dielectric layer I is on dielectric layer I-1 and on metal [layer] <u>plane</u> I-1 for I = 2, ..., N, and wherein the microvia structure electrically couples metal plane N to the metallic plane. metallic plane.

The present invention provides a method for forming an electronic structure, comprising:

providing an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

forming a redistribution structure including forming N dielectric layers denoted as dielectric layers 1, 2, ..., N, forming N metal planes denoted as metal planes 1, 2, ..., N, and forming a microvia structure through the N dielectric layers such that the microvia structure electrically couples metal plane N to the metallic plane, wherein N is at least 2, and wherein forming the N dielectric layers and the N metal [layers] <u>planes</u> includes setting a dummy index

J=0 and looping over J as follows:

adding 1 to J;

if J = 1 then forming dielectric layer 1 on the first surface of the substrate and on the metallic plane, else forming dielectric layer J on dielectric layer J-1 and on metal plane J-1;

forming metal plane J on dielectric layer J; and

if J < N then returning to adding 1 to J and continuing the looping, else ending the looping.

The paragraph beginning on page 13, line 4 has been amended as marked up in Appendix A and is as follows:

FIG. 2 illustrates advantages of the multiple redistribution layers (e.g., the redistribution layers **60**, **70**, **80**, and **90**) on the top surface **48** and on the bottom surface **49** of the substrate **10**. The redistribution layers serve as buildup layers which provides a capability of adding extra wiring layers; e.g., the metal planes **140-141** and **150-151**. The extra wiring level, coupled with the microvias (e.g, the microvias **132-135** and **144-148**) in the multiple redistribution layers, provide extra wireout capability for making more efficient use of space and increasing overall wiring density. In addition, there is increased flexibility in how electrically conductive structure may be distributed inasmuch as a metal plane on each redistribution layer may be any metal distribution, included a signal plane, a power plane, or a ground plane. With the multiple redistribution layers, any metal or metallic plane on a redistribution layer on the top surface **48** of the substrate **10** may be electrically coupled to any metal or metallic plane on a redistribution layer

on the bottom surface **49** of the substrate **10** or to any internal layer of the substrate **10**, in light of the electrically conductive paths facilitated by the microvias in the redistribution layers **60**, **70**, **80**, and **90** and the PTHs in the substrate **10**. FIG. 2 illustrates several of such electrically conductive paths. For example, the metal plane **140** is electrically coupled to the metal plane **151** through the path of the conductive region **137**, the microvia **133**, the conductive pad **42**, the PTH **32**, the conductive pad **45**, the microvia **135**, and the microvia **148**. As another example, the electronic device **110** is coupled to the conductive pad **44** of the PTH **31** by a path that includes the conductive pad **128**, the solder member **121**, the microvia **145**, the conductive pad **131**, the microvia **132**, the conductive pad **41**, the PTH **31**, and the conductive pad **44**. The electronic device **110** may be coupled to wiring in the redistribution layer **70** through the solder member **122** and the microvia **146**, or to wiring in the redistribution layer **60** through the solder member **120** and the microvia **144** or through the solder member **121** and the microvias **145** and **132**. The number and types of conductive paths facilitated by the multiple redistribution layers of the present invention are virtually unlimited. FIG. 3 also includes the aforementioned features and advantages.

The paragraph beginning on page 15, line 11 has been amended as marked up in Appendix A and is as follows:

As illustrated for the embodiments of FIGS. 2 and 3, the multiple redistribution structure on either the top surface **48** or the bottom surface **49** of the substrate **10** has N dielectric layers (denoted as dielectric layers 1, 2, ..., N) , N metal planes (denoted as metal planes 1, 2, ..., N), and a microvia structure, wherein $N \geq 2$. Dielectric layer 1 (i.e., redistribution layer **60** or **80**) is on the

top surface **48** or the bottom surface **49** of the substrate **10** and thus also on a metallic plane; i.e., on the metal plane **51** or the metal plane **52**, respectively. Thus, the metals planes **51** and **52** are each called a "metallic plane" for purposes of the notation being discussed herein. Metal plane 1 (i.e., metal plane **140** or **141**) is on dielectric layer 1, dielectric layer 2 (i.e., redistribution layer **70** or **90**) is on dielectric layer 1 and metal plane 1, metal plane 2 (i.e., metal plane **150** or **151**) is on dielectric layer 2, ..., dielectric layer N is on dielectric layer N-1 and metal plane N-1, and metal plane N is on dielectric layer N. The microvia structure electrically couples the metal plane N to the metallic plane (i.e., the metal plane **51** or the metal plane **52**) by a collection of microvias coupled with intervening metal planes. The microvia structure includes a microvia or a portion of a microvia through each of the N dielectric layers. Many such combinations of microvias are possible. An example microvia combination is N microvias (i.e., a microvia in each dielectric layer) such that microvia J is electrically coupled to microvia J-1 by metal plane J-1 for J=2, 3, ..., N. To illustrate, FIG. 3 has N=3 and shows: microvia **345** electrically coupled to microvia **385** by metal plane **380** (specifically, conductive pad **386** in metal plane **380**), microvia **385** electrically coupled to microvia **334** by metal plane **340** (specifically, conductive pad **338** in metal plane **340**), and microvia **334** electrically coupled to metal plane **51** by conductive pad **33**, which electrically couples the metal plane **395** to the metal plane **51** in light of the fact that conductive pad **346** of metal plane **395** is integral with, and thus electrically connected with, the conductive plating of the microvia **346**. Another microvia combination includes a microvia that passes through two or more dielectric layers (e.g., the microvia **144** of FIG. 2). For example and although not shown explicitly in FIG. 3, a microvia could pass through redistribution layers **360**, **370**, and **390**, or through redistribution layers **370** and **390**, just as microvia **144** of FIG. 2 passes through

redistribution layers **60** and **70**. Thus in FIG. 3, a microvia passing through redistribution layers **370** and **390** could be electrically coupled by metal plane **340** to a microvia (e.g., the microvia **332**, **333**, or **334**) in redistribution layer **360**.

In The Claims

Currently pending claims 1-25 are as follows, wherein claims 1, 2, 6, 19, and 22 have been amended as marked up in Appendix A;

1. (AMENDED) An electronic structure, comprising:

an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

a redistribution structure having N dielectric layers denoted as dielectric layers 1, 2, ..., N, N metal planes denoted as metal planes 1, 2, ..., N, and a microvia structure through the N dielectric layers, wherein N is at least 2, wherein dielectric layer 1 is on the first surface of the substrate and on the metallic plane, wherein metal plane J is on dielectric layer J for J =1, 2, ..., N, wherein dielectric layer I is on dielectric layer I-1 and on metal plane I-1 for I = 2, ..., N, and wherein the microvia structure electrically couples metal plane N to the metallic plane.

2. (AMENDED) The electronic structure of claim 1, wherein the microvia structure includes N microvias denoted as microvias 1, 2, ..., N, wherein the microvia K passes through dielectric layer K for K = 1, 2, ..., N, wherein metal plane N is electrically coupled to microvia N, wherein metal plane J-1 electrically couples microvia J to microvia J-1 for J = 2, 3, ..., N, and wherein microvia

1 is electrically coupled to the metallic plane.

3. The electronic structure of claim 1, wherein the microvia structure includes a microvia that passes through the N dielectric layers, wherein the microvia electrically couples metal plane N to the metallic plane.

4. The electronic structure of claim 1, wherein the microvia structure includes a first microvia, wherein the first microvia passes through dielectric layers M through N, wherein M is at least 2, wherein N is at least 3, wherein M is less than N, and wherein metal plane N is electrically coupled to the first microvia.

5. The electronic structure of claim 4, wherein the microvia structure further includes a second microvia that passes through dielectric layers 1 through M-1, wherein metal plane M-1 electrically couples the first microvia to the second microvia, and wherein the second microvia is electrically coupled to the metallic plane.

6. (AMENDED) The electronic structure of claim 4, wherein the microvia structure further includes M-1 second microvias denoted as second microvias 1, 2, ..., M-1, and wherein the second microvia K passes through dielectric layer K for K = 1, 2, ..., M-1, wherein the metal plane M-1 electrically couples the first microvia to second microvia M-1, wherein if M > 2 then metal plane J-1 electrically couples second microvia J to second microvia J-1 for J = 2, 3, ..., M-1, and wherein second microvia 1 is electrically coupled to the metallic plane.

7. The electronic structure of claim 1, wherein N = 2 or N = 3.

8. The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a stiffness of at least about 700,000 psi.

9. The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a glass transition temperature of at least about 150 °C.

10. The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a coefficient of thermal expansion of no more than about 50 ppm/°C.

11. The electronic structure of claim 1, wherein at least one of the metallic plane and the N metal planes includes a signal plane.

12. The electronic structure of claim 1, wherein at least one of the N metal planes includes a power plane.

13. The electronic structure of claim 1, wherein at least one of the N metal planes includes a ground plane.

14. The electronic structure of claim 1, wherein the substrate includes a dielectric material comprising a polytetrafluoroetheylene (PTFE) having silicon particles therein.

15. The electronic structure of claim 14, wherein the substrate further includes a ground plane, a power plane, and a signal plane, wherein the ground plane, the power plane, and the signal plane are each embedded within the dielectric material, and wherein the signal plane is disposed between the ground plane and the power plane.

16. The electronic structure of claim 14, wherein the substrate further includes a ground plane, first and second power planes, and first and second signal planes, wherein the ground plane, the first and second power planes, and the first and second signal planes are each embedded within the dielectric material, wherein the first signal plane is disposed between the ground plane and the first power plane, and wherein the second signal plane is disposed between the ground plane and the second power plane.

17. The electronic structure of claim 1, further comprising an electronic device electrically coupled to the metal plane N by a solder member.

18. The electronic structure of claim 17, wherein the electronic device includes a semiconductor chip.

19. (AMENDED) The electronic structure of claim 17, wherein the electronic structure includes at least one power plane, and wherein a thickness of the redistribution structure is large enough that a nearest distance between the solder member and any power plane of the at least one power plane is not less than a predetermined minimum distance value.

20. The electronic structure of claim 19, wherein the predetermined minimum distance value is predetermined by requirements of a given radio frequency application.

21. The electronic structure of claim 1, wherein a plated through hole (PTH) passes through the substrate from the first surface to a second surface of the substrate, and wherein the metallic plane is electrically coupled to the PTH.

22. (AMENDED) The electronic structure of claim 21, further comprising a second metallic plane on the second surface of the substrate and a second redistribution structure having P second dielectric layers denoted as second dielectric layers 1, 2, ..., P, P second metal planes denoted as second metal planes 1, 2, ..., P, and a second microvia structure through the P second dielectric layers, wherein P is at least 1, wherein second dielectric layer 1 is on the second surface of the substrate and on the second metallic plane, wherein second metal plane J is on second dielectric layer J for J =1, 2, ..., P, wherein if I > 1 then second dielectric layer I is on second dielectric layer I-1 and on second metal plane I-1 for I = 2, ..., P, wherein the microvia structure electrically couples the second metal plane P to the second metallic plane, and wherein the second metallic plane is electrically coupled to the PTH.

23. The electronic structure of claim 22, wherein P = N.

24. The electronic structure of claim 22, further comprising an electronic board electrically coupled to the second metal plane N by a solder member.

25. The electronic structure of claim 24, wherein the electronic board includes a circuit card.

REMARKS

Claims 1-25 are currently pending, wherein claims 1, 2, 6, 19, and 22 have been amended for improving clarity and not in response to any rejection in the Office Action mailed 07/05/02. Claims 26-50 are withdrawn.

The Specification has been amended for improving clarity and the amendments to the Specification is fully supported by the originally submitted specification, drawings and claims, so that no new matter is believed to have been added.

The Examiner rejected claims 6 and 22 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The Examiner rejected claims 1-25 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants respectfully traverse the §112 rejections with the following arguments.

35 U.S.C. §112, First Paragraph

With respect to claims 6 and 22, the Examiner alleges that "[b]y using the term 'if', it is unclear as to the number of layers in the device and scope of the invention." In response,

Applicants note that the feature "if $M > 2$ then metal plane J-1 electrically couples second microvia J to second microvia J-1 for $J = 2, 3, ..., M-1$" in claim 6 is a conditional limitation on the scope of claim 6 such that the limitation of "metal plane J-1 electrically couples second microvia J to second microvia J-1 for $J = 2, 3, ..., M-1$" is conditioned on M exceeding 2. Applicants respectfully contend that a conditional limitation appearing in a claim is most certainly proper and that the Examiner has not cited any recognized authority to support a contention that a conditional limitation in a claim violates 35 U.S.C. §112, First Paragraph.

For clarity with respect to claim 6, Applicants point out that the number of layers (N) in the redistribution structure and the number of layers (N-M+1) encompassed by the first microvia can be easily calculated from the values of N and M which are variables. For example, claim 4 (from which claim 6 depends) states the conditions of $M\geq2$, $N\geq3$, and $M<N$, and the conditionality of "if $M > 2$ ..." in claim 6 changes the aforementioned conditions to $M\geq3$, $N\geq4$, and $M<N$, respectively, which is clear and unambiguous. Additionally, the conditions of $M\geq3$ and $N\geq4$ in claim 6 is clearly within the scope of the conditions $M\geq2$ and $N\geq3$ in claim 4.

For clarity with respect to claim 22, Applicants point out that it is very clear from the language of claim 22 that the number (P) of second dielectric layers satisfies $P\geq1$, and the condition "if I>1 ..." pertains to the case of $P\geq2$ which is clearly within the scope of $P\geq1$.

Based on the preceding arguments, Applicants respectfully maintain that the rejection of claims 6 and 22 under 35 U.S.C. §112, First Paragraph is improper.

35 U.S.C. §112, Second Paragraph

The Examiner alleges that "[w]ith respect to claim 1, it is ambiguous how the word

circuitized further limits the scope of the term 'substrate'." In response., Applicants respectfully note that the term "circuitized substrate" identifies a substrate that is circuitized and therefore is more narrow than "substrate" since a substrate may or may not be circuitized. Thus, "substrate" is broader that "circuitized substrate." Applicants respectfully point out that the United States Patent and Trademark Office has allowed many patents to issue which includes "circuitized substrate" in the claims including, *inter alia*, the following four patents during the month of September 2002: United States Patent 6,455,924 (Alcoe et al., issued September 24, 2002); United States Patent 6,455,785 (Sakurai et al., issued September 24, 2002); United States Patent 6,455,139 (Konrad et al., issued September 24, 2002); United States Patent 6,477,914 (Angelopoulos et al., issued September 10, 2002); etc. Thus the Examiner's rejection is contrary to accepted practice by the United States Patent and Trademark Office. Accordingly, Applicants respectfully maintain that the aforementioned rejection of claim 1 under 35 U.S.C. §112, Second Paragraph is improper.

The Examiner alleges that "[f]urther, there is no antecedent basis for: dielectric 1, dielectric I, dielectric I-1, dielectric K, metal plane J, metal j-1, mircrovia J, metal plane N, dielectric layers M, dielectric N, dielectric M-1, dielectric K, metal plane M-1, metal plane j-1, microvia J, microvia 1, P second dielectric, second dielectric layer 1." In response., Applicants respectfully note that this rejection is improper because the Examiner has not stated which claims are being rejected. Applicants respectfully emphasize that the amendments to claims 1, 2, 6, 19, and 22 are for improving clarity only and not in response to the aforementioned rejection which Applicants contend is improper.

The Examiner alleges that "[c]laims 1-25 have not been rejected over the prior art because, in light of the 35 U.S.C. §112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. See also MPEP 2173.06." In response, Applicants respectfully contend that the limitations and scope of claims 1-25 is clear and unambiguous. Thus Applicants respectfully request that the Examiner conduct a search of the prior art and that the next Office Action reflect the result of said search of the prior art.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-25 meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

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